

[illegible]

CP2102N-A02-GQFN24

3V3

GND

C1 10uF

C2 100nF

R3 1K

7 VREGIN

6 VDD

5 VIO

4 VUSB\_DET

3 USB\_DM

2 USB\_DP

1 RSTb

25 GND

16 NC

10 NC

2 GND

19 RTS

23 DTR

20 STM32\_TX

21 STM32\_RX

1 RI/CLK

19 CTS

22 DSR

24 DCD

15 SUSPENDb

14 SUSPEND

11 GPIO3/WAKEUP

12 GPIO2/RS485

13 GPIO1/RXT

14 GPIO0/TXT

LED\_RXD

LED\_TXD

R11 1K8

R13 1K8

D2 BLUE 5mcd 0.5mA 2.4V

D3 BLUE 5mcd 0.5mA 2.4V

U2

Pin	Function	Module Pin	Module Pin
1	GND	PPCC062LFBN-RC	
2	3V3 (OUTPUT ONLY)	GND	2, 3V3
3	RESET (ACTIVE LOW)	RESET	3, 4 SPI2_SCK
4	SPI2_SCK	SWCLK	5, 6 SPI2_MISO
5	GPIO (PA14) / SWCLK	SWDIO	7, 8 SPI2_MOSI
6	SPI2_MISO	I2C1_SCL	9, 10 USART2_TX
7	GPIO (PA13) / SWDIO	I2C1_SDA	11, 12 USART2_RX
8	SPI2_MOSI		
9	I2C1_SCL		
10	GPIO (PA2) / ADC1_IN7 / USART2_TX		
11	I2C1_SDA		
12	GPIO (PA15) / USART2_RX		

J5

The circuit diagram illustrates the 32-bit parallel bus interface for the STM32F407VGT6. It features four input signals: DTR, RTS, BOOT0, and RESET. DTR and RTS are connected to the D+ and D- pins of a 32-bit parallel bus (Q1, Q2) via 20k resistors (R1, R2) to GND. BOOT0 is connected to the BOOT pin of a 32-bit parallel bus (Q3) via a 20k resistor (R6) to 3V3. RESET is connected to the RESET pin of a 32-bit parallel bus (Q4) via a 20k resistor (R7) to 3V3 and a 100nF capacitor (C4) to GND. A switch (SW1) is connected to the RESET pin and GND. The output of the 32-bit parallel bus is connected to the D+ and D- pins of a 32-bit parallel bus (Q5, Q6).

DTR	RTS	BOOT0	RESET
0	0	0	1
1	1	0	1
0	1	0	0
1	0	1	1

Note: For more details open the file audio-simulation.asc in LTspice

3V3

D7 RGB

RGB\_R RGB\_G RGB\_B

LED\_R LED\_G LED\_B

R25 R23 R22

1K 1K8 240

25mcd 25mcd 25mcd

1.4mA 0.6mA 2.5mA

1.9V 2.4V 2.7V

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